Q.P. Code: 16EC417 **R16**

Reg. No: | | | | | | | | | | |

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY:: PUTTUR

(AUTONOMOUS)

B.Tech III Year I Semester Supplementary Examinations November-2020

LINEAR IC APPLICATIONS

(Common to EEE & ECE)

Time: 3 hours Max. Marks: 60

(Answer all Five Units **5 x 12 = 60** Marks)

UNIT-I

1		Calculate the amplification factor for AC signal input in dual input balanced output differential amplifier.	**12M**

OR

2	**a**	Explain how the constant current bias circuit is replaced by the current mirror circuit.	**6M**
	b	Explain and derive the current expression of current mirror circuit diagram	**6M**

UNIT-II

3		Explain in detail about external frequency compensation techniques with neat sketches.	**12M**

OR

4	**a**	Explain the importance of the stability criterion of the op-amp.	**6M**
	b	Define the total input offset voltage and thermal drift.	**6M**

UNIT-III

5		Draw the circuit diagram of the instrumentation amplifier and derive the gain.	**12M**

OR

6		Explain the operation of first order low pass butter worth filter & derive the expression for filter gain & draw a neat sketch of frequency response.	**12M**

UNIT-IV

7	**a**	Explain the comparator and zero crossing detector.	**6M**
	b	Explain the operation of Schmitt trigger. Discuss its characteristics & limitations.	**6M**

OR

8	**a**	Using op-amp, explain how to generate a triangular wave from the square wave.	**6M**
	b	Explain the operation of Wein bridge oscillator and derive its frequency expression with neat circuit diagram.	**6M**

UNIT-V

9		Draw the circuit diagram of single Slope ADC and explain its working with neat sketches.	**12M**

OR

10	**a**	Draw and explain the weighted resistor DAC.	**6M**
	b	Explain ladder type DAC with a neat circuit diagram.	**6M**

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